A 1-V 2GHz VLSI CMOS Low Noise Amplifier

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ABSTRACT — **A new LNA topology is presented in this paper. Compatible with VLSI technology the architecture is dedicated to the UMTS third generation mobile phone. Operating under 1V supply voltage the circuit provides a more than 11 dB gain at 2.1 GHz. With a −11 dBm ICP1, the power consumption is lower than 4 mW, making the architecture well suited to very low power applications. The noise figure of 1.8 dB takes advantage of the inductive degeneration technique. The 0 dBm IIP3 fulfils the UMTS requirement whose the circuit is dedicated to.**

I. INTRODUCTION

CMOS integrated circuits for wireless applications in the 2 GHz frequency range are receiving much attention due to their potential for low cost and the prospect of system level integration. A key building block for the RF front-end is the low noise amplifier (LNA) which precedes a high noise stage (e.g. image-reject filter or mixer), and plays a critical role in determining the over all noise figure (NF) of the receiver.

From a performance viewpoint, to be competitive with bipolar or even GaAs, CMOS LNA's must equal or surpass the low power consumptions and low noise figure of these technologies. From a cost point of view, the LNAs' should be implemented in a standard digital CMOS technology requiring a minimal number of external components. While recent works have demonstrated the potential of CMOS LNAs' for 2 and 5 GHz applications [1], an underlying problem tends to limit this growth: the supply voltage. At present the down scale rule of CMOS gate length leads the designers to operate under 1V. In this case it comes to be difficult to reach good performances. In this paper is presented an architecture suitable to operate at low voltage while maintaining the previously presented behavior.

The first section presents two techniques used to achieve the architecture. Then the circuit design is depicted in the following section. The third section presents the measurement results and the last one gives some conclusions and perspectives about this new topology.

II. PRINCIPLE

The various techniques brought into play are described in this section. By combining the reuse and degeneration techniques we've managed to design a new topology well suited to low voltage, low power applications.

A The reuse technique

It is well known that reuse technique [2] is dedicated to reduce current consumption as it is depicted in Fig.1.

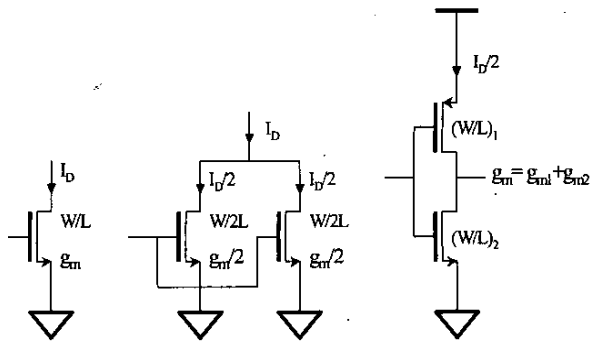

Fig 1. The current reuse technique

Thanks to the NMOS and PMOS stacked stage, we kept the same transconductance g_m with half the current. However, from an analog point of view, the high output impedance can be used to provide gain, an interesting behavior for LNA design. Nevertheless this advantage is also a drawback due to its output unsteady DC operating point. So we take advantage of a DC-Common Mode FeedBack loop (CMFB) as depicted in Fig.2. Indeed the CMFB collects the DC output and enslaves the DC input in order to control the LNA DC stability.

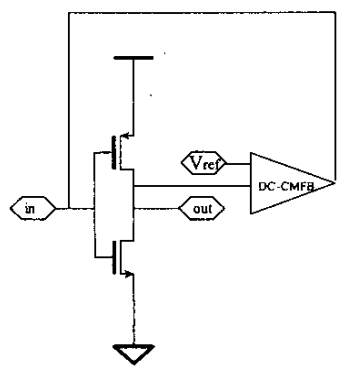

Fig 2. The feedback configuration

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B the inductive degeneration

A common though efficient LNA topology [3] is depicted in Fig.3:

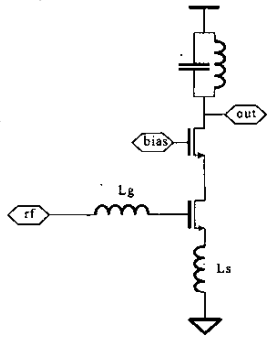

Fig 3. Folded cascode with inductive degeneration [3]

The use of inductive degeneration through L_s has the benefit of simultaneously achieving both input and noise matching. As far as matching is a matter of concern, the Ls inductance seems like a real impedance equals to Ls.gm/Cgs at operating frequency that allows the designer to match the 50Ω input. Lg is used to cancel the Cgs capacitor. So the maximum signal is collected and gain could be optimized. From the noise figure point of view, the size of the input transistor is chosen to minimize it as depicted in the following expressions [4] :

$$F_{\min} = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma . \delta . (1 - |c^2|)}$$

with $\omega_T = g_m / Cgs$ the transition pulsation, g_m the transistor transconductance, C_{gs} the gate source capacitor. $\gamma = 3/2$ is the channel thermal noise. C is the correlation term equals to j0.395. δ is the coefficient of gate noise. Thus we can derive the previous expression in order to calculate the optimal transistor size at the frequency of interest:

$$W_{opt} = \frac{1}{3\omega . L . C_{ox} . R_s}$$

with R_s=50Ω and L is the gate length.

Assuming $\omega < \omega_T$ the Fmin expression is effective and shows that the higher the frequency the higher the NF. Fortunately, thanks to the down scale rule of CMOS length gate, the ω_T parameter raises up and allows us to operate at high frequency while maintaining good noise figure. Owing to this technique, the critical first stage of a CMOS LNA is efficient. Obviously, this results can only be obtained for a narrow frequency band.

III. THE CIRCUIT DESIGN

The implemented circuit is presented in Fig.4. It is composed of three parts:

- the first one is the LNA core presented in the previous section. All the passive components are integrated except for the inductance Lg which cancels the two input Cgs capacities. Due to the large gain achieved by the circuit the miller effect links the input matching to the output load. Thus it becomes difficult to realize 50Ω input matching and the Lg value is not exactly the one noise optimization forecasts.

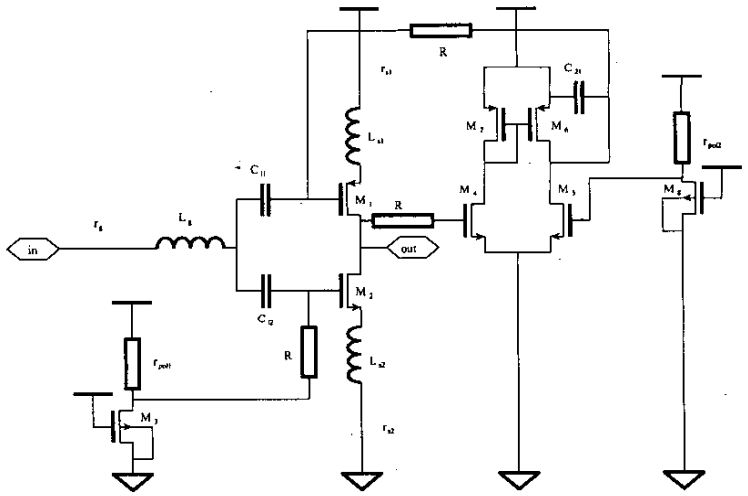

Fig 4. circuit design

Furthermore the dynamic voltage lost across the parasitic resistance of inductance Ls can't be neglected under 1V supply voltage. These ones reduce the $|V_{GS}|$ command thus the current, the gain and moreover add thermal noise.

- the second part is the DC-CMFB realized with a differential pair which acts like a low pass filter thanks to the weak biasing of the transistors. A RC low-pass filter is set up with C_{21} in order to strengthen the low frequency cutoff behavior of the feedback which prevents the instability of the circuit.

- the last part is the bias cell built with the PN junction of a PMOS transistor and a resistor. This topology is suited to 1V supply voltage. Owing to the large width of the transistor, one manage to provide a roughly steady voltage reference.

IV. THE MEASUREMENT RESULTS

This circuit was implemented in a CMOS VLSI 0.18 µm technology. A FR4 PCB was manufactured with just micro strip lines and microwaves boarding techniques such as separated ground filled area. The chip micrograph is depicted in Fig. 5, the LNA size is 175µm*50µm. Obviously the first advantage of this architecture is its weak silicon area needed to be set up.

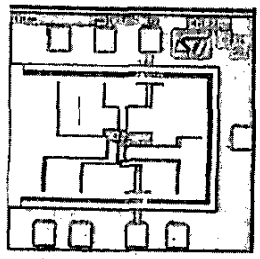

Fig 5: chip micrograph

Except for L_g inductance no additional off chip component is added in order to limit the leakage, hot ports are laid in the sixth metal level so as to reduce the resistance access and are connected via no ground-shield pad to the chip reducing the parasitic capacitors in this way.

The voltage gain curve versus supply voltage depicted in Fig.6 shows that the architecture and so the size of the transistors is well suited to operate under 1V. Obviously 11 dB maximum gain is reached for this value testifying the good matching of the double inductive degeneration at the frequency of interest and under forecasted biasing conditions.

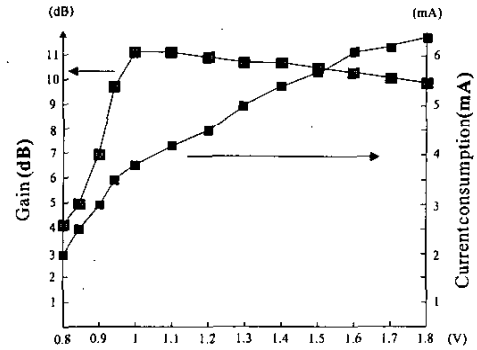

Fig 6. gain and consumption versus supply voltage

Using QPSK modulation, UMTS standard needs high linearity involving strict constrains on circuit. Depicted in Fig 7, the 1 db compression point expresses the limit to linear operation. One can observe that the topology brought into play affords a pretty good linearity with a –11 dBm ICP1 without overconsuming, the current consumption is 3.8 mA.

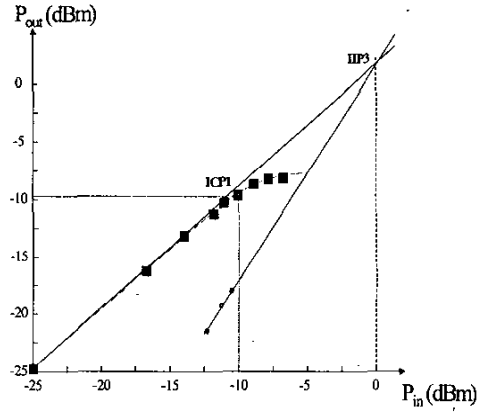

Fig 7. ICP1 and IIP3

Another relevant attribute of the front end is its ability to handle large signals without armful distortion. Reported on the Fig 7 we notice that the 0 dBm IIP3 fulfils the UMTS requirement [5]. Thus excellent linearity is obtained despite the 1 V supply voltage that usually reduces gain and linearity. Moreover the stringent UMTS features are fully satisfied.

Measured at the frequency of 2.1 GHz with a HP8970B noise figure meter, the NF is found to be 1.8 dB. This good result is reached thanks to the inductive degeneration set up with the bonding wire. This result confirms that the NF optimization of [3] matched to the reuse architecture is efficient. Thus the 9 dB UMTS noise figure requirement for LNA is achieved successfully by this circuit [5].

Nevertheless it is well known that gain and noise figure require a good S_{11} input matching. In fact this key parameter allows to collect maximum signal thus best gain can be achieved and so good linearity. As far as noise is concerned, the noise optimization leads to provide a good 50 Ω input matching. In our case it means to control inductive degeneration through L_g and L_s values. One can observe in fig 7 that S_{11} reaches –24.5 dB at 2.0 GHz that is excellent. Moreover due to the fact that no tuned load are used in the circuit its bandwidth is solely defined by the input matching bandwidth thus the LNA bandwidth is as large as 750 MHz.

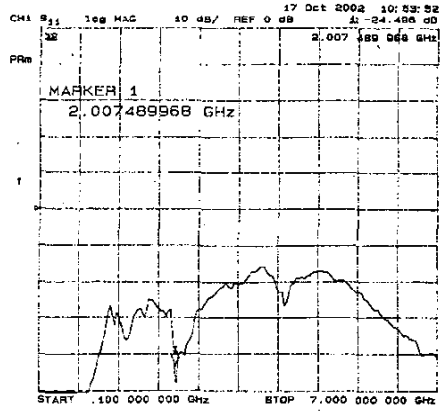

Fig 8: S_{11} parameter

From the output matching view point due to the fact that the LNA is dedicated to be connected to an integrated mixer the 50Ω output matching is not required. Thus leading a high output impedance the S_{22} parameter measurement is not significant.

All the measurement results are summarized in Table 1. We can notice that these ones are well suited to fulfil the stringent UMTS features while the circuit operates under 1V supply voltage.

V. CONCLUSION

This paper presents a 2.1 GHz single-stage LNA with a 1.8 NF consuming 3.8 mA. Operating under 1V supply voltage the circuit provides a 11 dB gain whith a –11 dBm 1 dB compression point. Implemented in a 0.18 µm CMOS VLSI technology, this LNA is well suited to achieve amplification in modern RF receiver which requires designer to provide fully integrated and low power consumption architectures for SoC applications. From both performance and cost standpoint these results show that CMOS is very competitive with silicon bipolar and SiGe [6, 7] technologies. Additionally, as technologies shrinks f_T will increase, thus better NF performance will be achieved at the same power consumption and gain.

TABLE 1.
MEASUREMENT RESULTS

Frequency	2 GHz
Supply voltage	1 V
Current consumption	3.8 mA
Gain	11 dB
Noise figure	1.8 dB
ICP1	-11 dBm
IIP3	0 dBm
S_{11}	-25 dB
Technology	0.18 µm
Bandwidth	750 MHz

VII. REFERENCES

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